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**Project** – Classical PLL

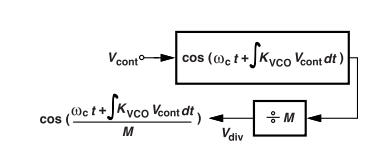
**VCO and Divider behavioral**

**Theory:**

When we simulate the behavioral model of VCO and divider, we get less simulation time in cadence so we use this model for simulation of PLL in this experiment.

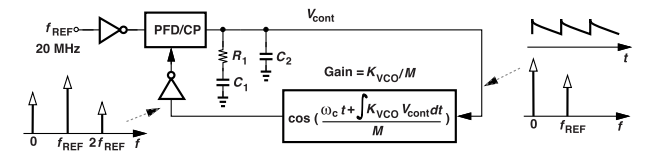
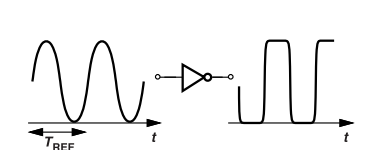
**Circuit Diagrams:**

1. A VCO can be represented by sinusoidal function with integral phase as shown below



**Fig.1: Block Diagram of a VCO and the Divider using equations.**

1. Complete PLL with VCO & Divider as a VerilogA code. The two inverters have been used to convert the sinusoidal into an almost square waveform required by the PFD. In some cases, a cascade of multiple inverters might be needed to get waveform sufficiently close to the square wave.

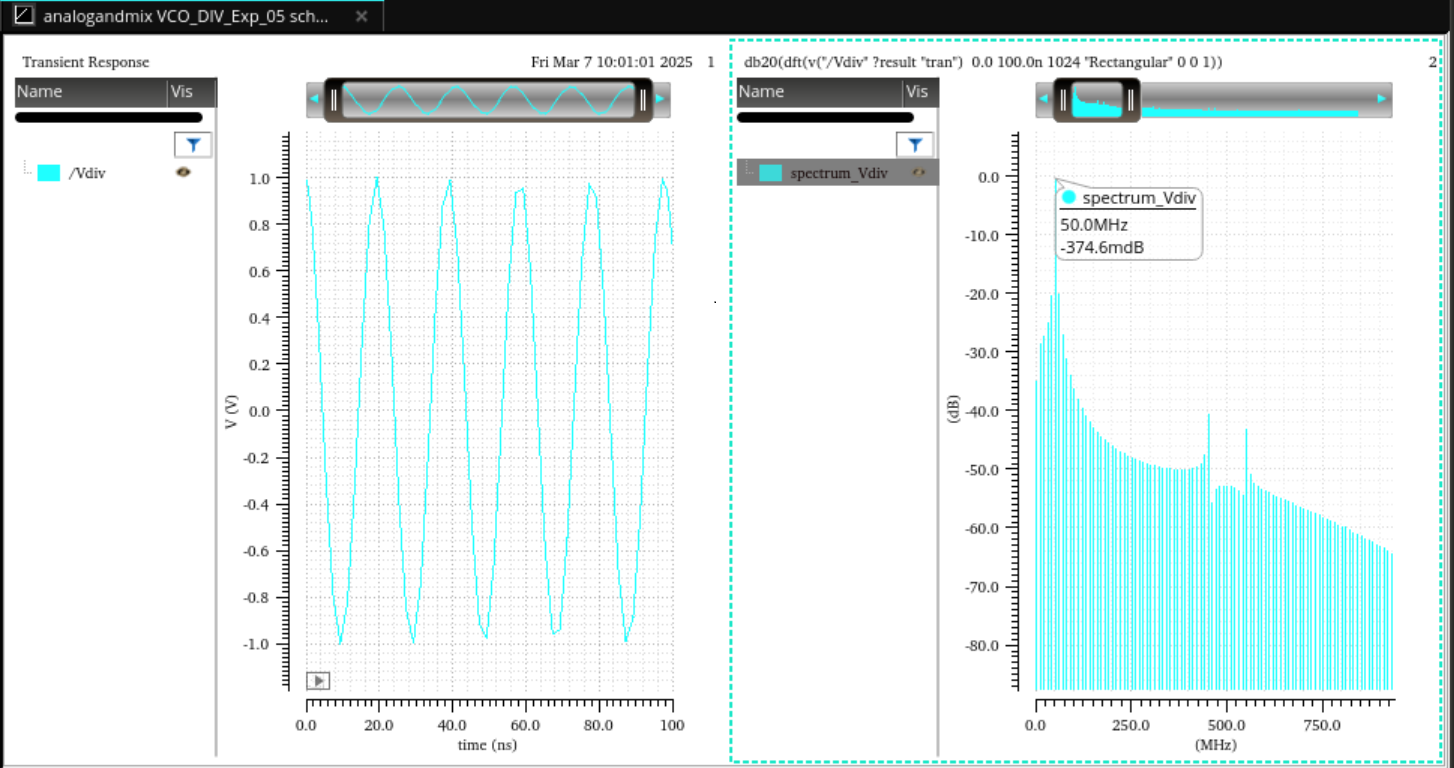
 

**Fig.2: (a) Complete PLL with VCO and divider . (b) A sinusoidal wave followed by an inverter.**

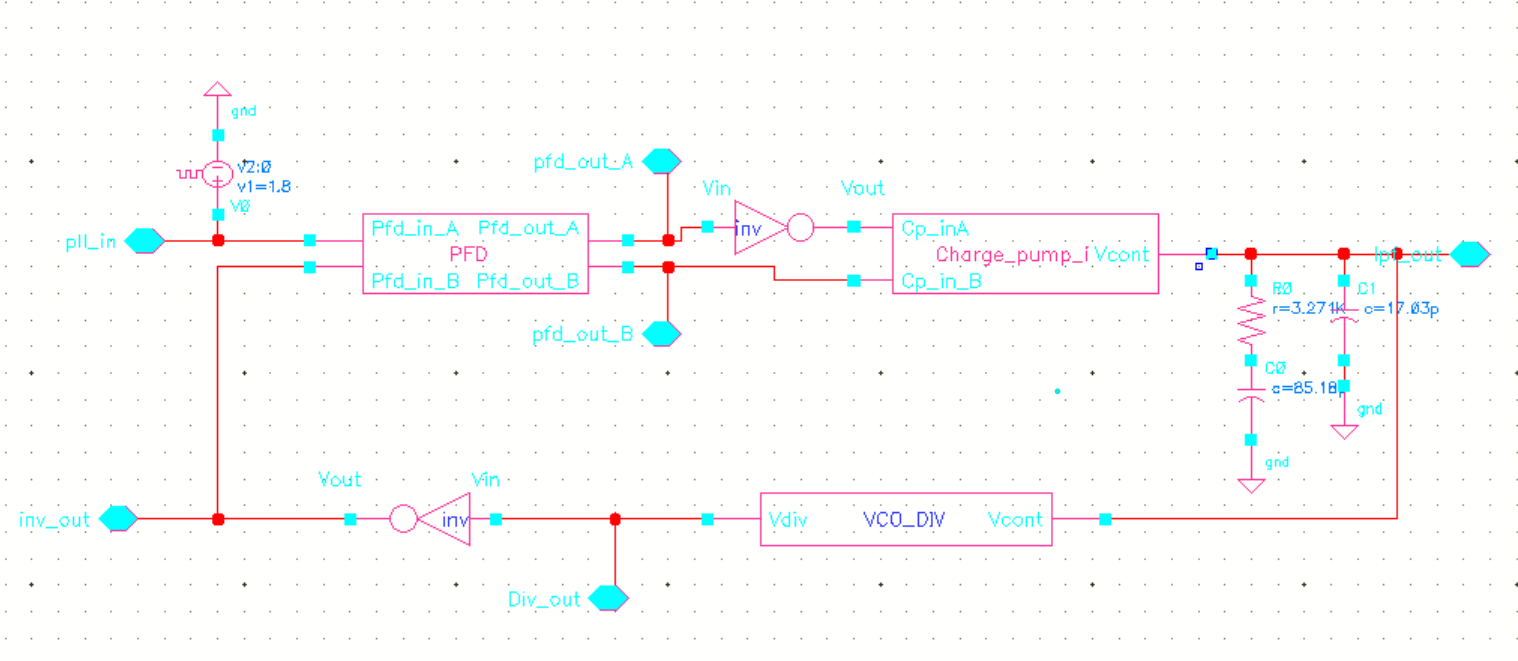
**PLL Design:**

1. Given: fr = 24Mhz, fo= 1.152GHz, ζ= 1, ωbw= ωr/10, Kvco= 2.1061Ghz/V, Ip= 100μA
2. Find the Divider M, the loop filter elements R1,C1and C2.

**Output :**

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**Fig 1 :** Output waveform of VCO and divider block (stop time =0.1 us and Vcont=1V) with ref frequency = 50 MHz

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**Fig 2:** Schematic of complete PLL using Behavioral VCO and Divider Block

From calculation, I get

C1 = 85.18 pF

C2 = 17.03Pf,

R1 = 3.271 Kohm,

Kvco = 2.1061 GHz /V

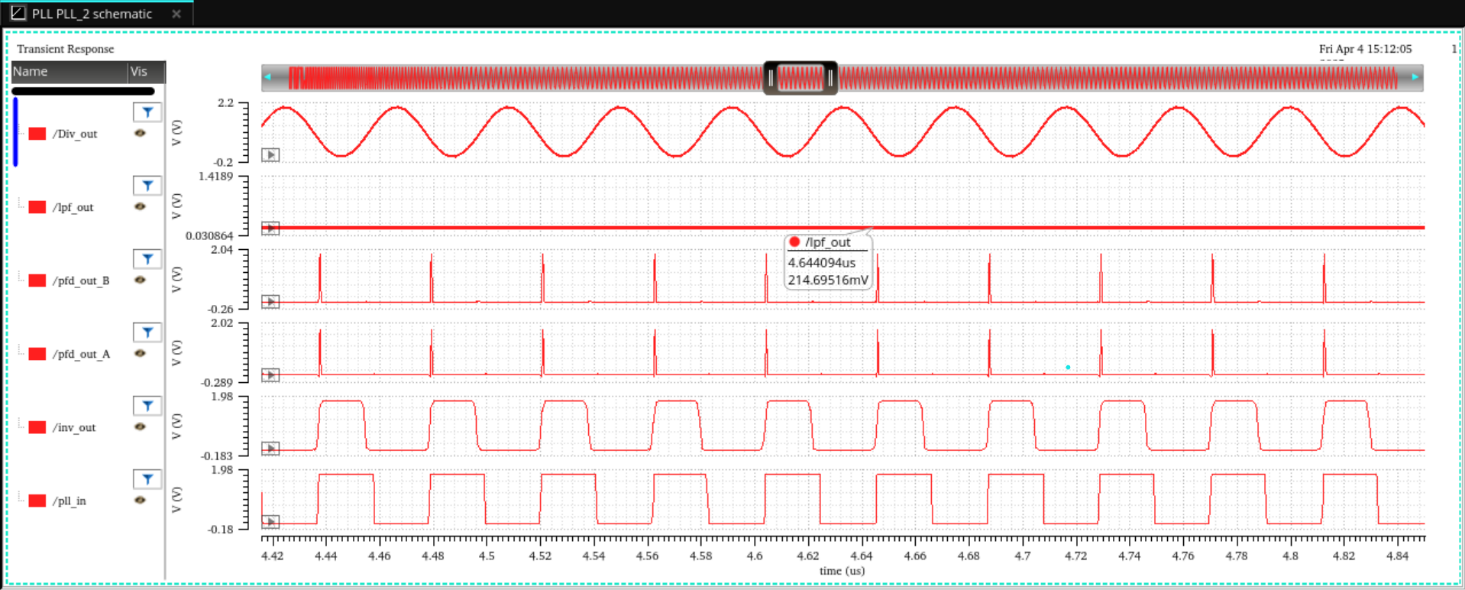


Fig 3: Output waveform of PLL

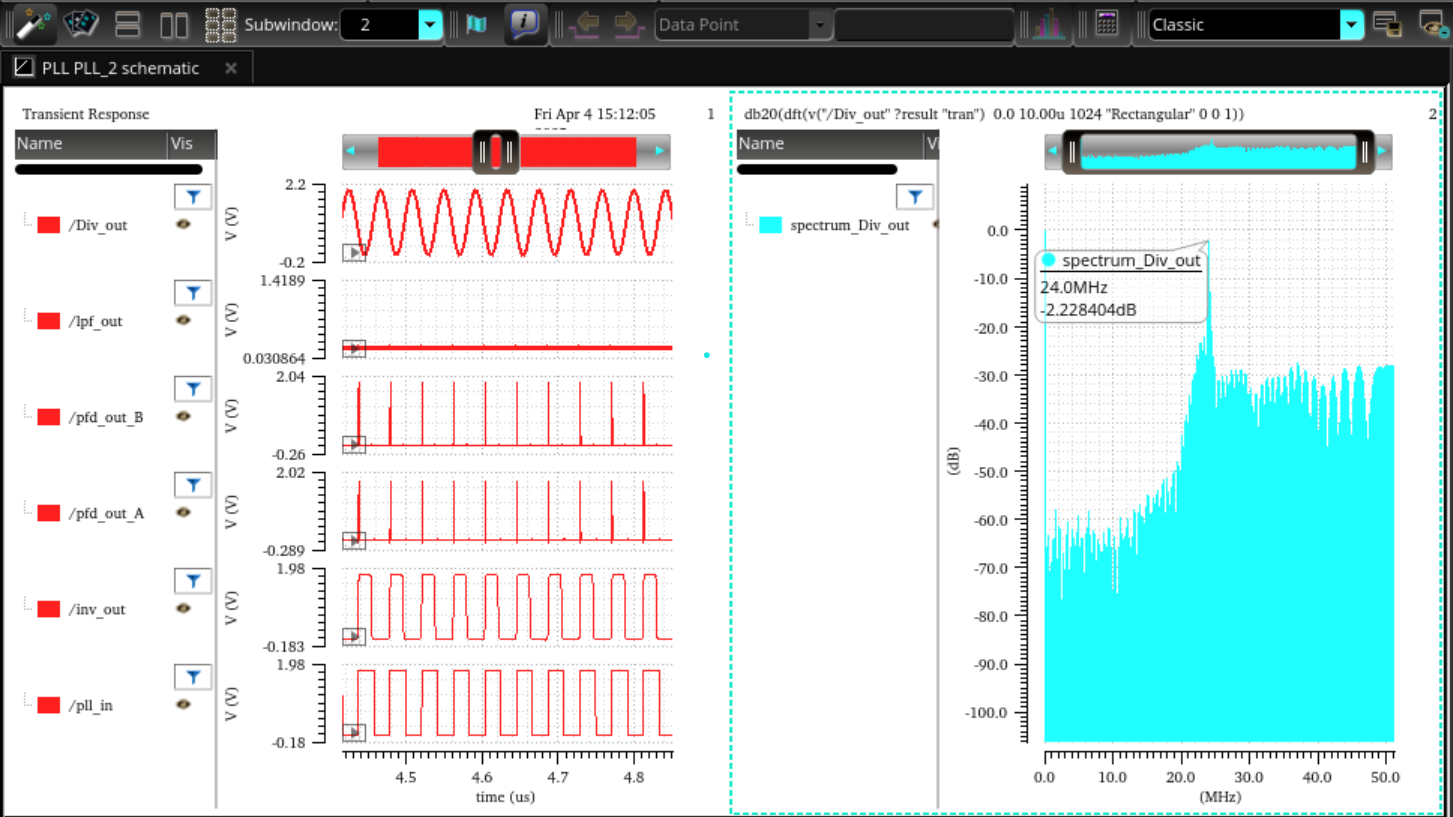


Fig 4: Output frequency of VCO and Divider block